Quantifying Risk using Probabilistic Circuits

MASSIVELY PARALLEL, HARDWARE-ACCELERATED MONTE CARLO METHODS FOR SCALABLE NUCLEAR SAFETY ANALYSIS

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NUCLEAR SAFETY ANALYSIS requires robust risk estimates that account for complex failure scenarios. This research presents a data-parallel Monte Carlo framework that models both success and failure scenarios in a single pass, harnessing graphics processors to handle millions of random draws. Benchmarks against traditional PRA tools show orders-of-magnitude speedup for large risk models, while maintaining accuracy. While slow convergence for rare events remains a challenge, advanced sampling strategies offer solutions. Future work will incorporate common-cause dependencies and adaptive variance reduction to further enhance accuracy and efficiency.

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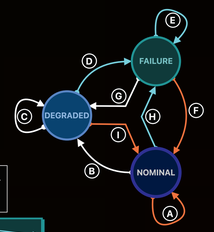
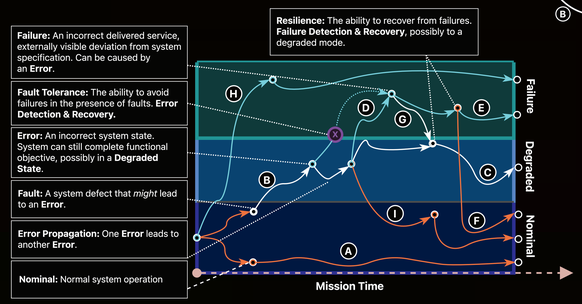
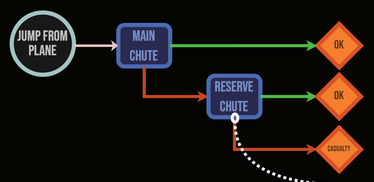
SOURCE CODE

① Nuclear Safety & Probabilistic Risk Assessment

The two blue diagrams (right, below) illustrate how a system can transition from nominal to degraded or outright failure over time. Probabilistic Risk Assessment (PRA) models and quantifies these transitions to calculate the overall likelihood of undesired outcomes. Efficiently and accurately estimating the probability of such events is the key focus of this research.





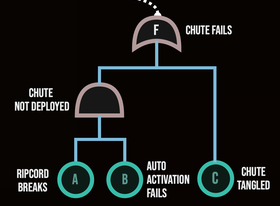


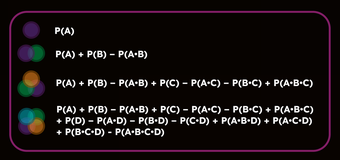
A SCENARIO-BASED APPROACH

Event trees split an initial trigger into branching pathways, each reflecting a possible outcome. The parachute example shows how main and reserve chutes combine to produce different success or failure endstates.

LOGICAL FAULT DECOMPOSITION

A fault tree outlines how component-level faults (e.g., tangled chute, broken ripcord) logically combine to produce a top-level failure (e.g., "Chute Fails"). Gates like AND/OR capture whether multiple faults must happen together or if any single fault suffices.

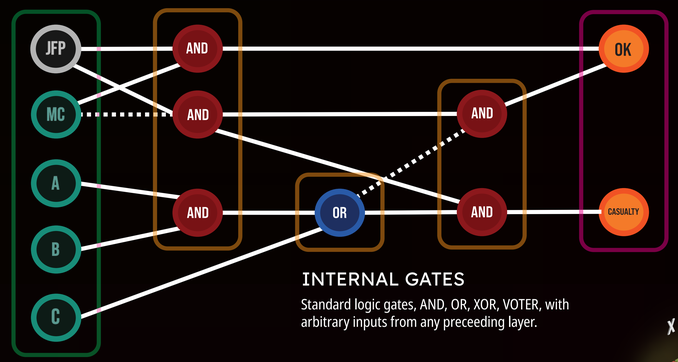




INCLUSION-EXCLUSION

Probabilities are computed using the inclusion-exclusion principle. Enumerating every subset of faults quickly becomes unmanageable as systems grow.

② From Risk Models to Probabilistic Circuits



TALLIES

All True/1 logic evaluations are summed to develop a tally. Dividing by the total samples gives an estimate for the expected value.

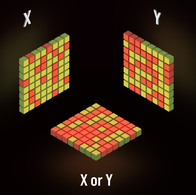
INTERNAL GATES

Standard logic gates, AND, OR, XOR, VOTER, with arbitrary inputs from any preceeding layer.

PROBABILISTIC INPUTS

Samples are drawn based on each event's probability distribution.

Linked event trees and fault trees are transformed into a layered directed acyclic graph using a modified topological sort. Negations are expressed as dashed edges. The underlying Boolean expression remains unchanged. Additional manipulations, such as reductions or expansions are not strictly necessary. The graph is traversed by layer. All nodes in a layer execute simultaneously. Bits can be packed into larger datatypes for maximum throughput. Traversal over the constructed probabilistic circuit is reduced into a single, hardware-accelerated pipeline. By encoding component failures in compact bit vectors, modern GPUs, and multicore CPUs can evaluate logic for massively parallel calculations.

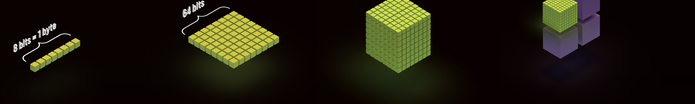


A BITWISE-OR

Above: Bitwise operations are applied for the OR logic over the entire double word in parallel, maximizing throughput.

PER-INSTRUCTION SCALING

A single bitwise instruction can operate on anywhere between a byte to 2048 bits per call, depending on hardware.



A BYTE
The smallest operand size for modern x86, ARM processors.

A WORD
A 64-bit double word, the largest operand for general purpose registers/instructions.

A CHUNK
512 bits. The maximum size currently supported by x86-64 CPUs using the AVX2/AMX instruction set.

A WARP
32 threads simultaneously work on 64-bit operands, providing 2048 bits of throughput. Available on NVIDIA GPUs.

③ Case Study & Benchmarks

DATASET COMPOSITION

The Aralia collection consists of 43 distinct fault trees, each with varying numbers of basic events (BEs), gate types (AND, OR, K/N, XOR), and minimal cut-set counts.

DIVERSE PROBLEM SIZES

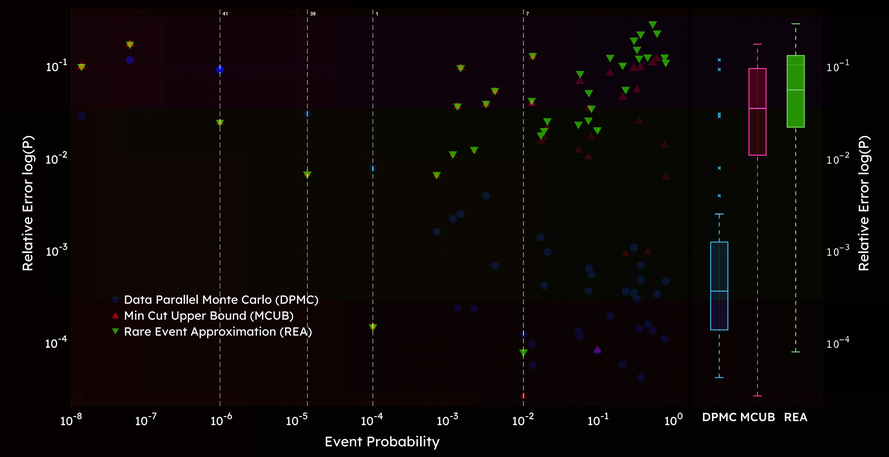
Small trees (e.g. 25–32 BEs) through large models with over 1,500 BEs.

WIDE PROBABILITY RANGE

Top-event probabilities spanning from rare events to fairly likely failures with probability above 0.7.

MODEL VARIABILITY

Some trees are primarily AND/OR, others incorporate more advanced gates (K/N, XOR, NOT), providing thorough coverage of typical (and atypical) fault tree logic structures.



Here, we compare our proposed method, Data Parallel Monte Carlo (DPMC), along with the Min Cut Upper Bound (MCUB), and the Rare Event Approximation (REA) across probabilities from 10^{-8} to 10^{0}. DPMC performs accurately over the full range, while MCUB and REA can miss true probabilities when events become extremely rare or non-rare. The chart shows relative error distributions, illustrating how massively parallel sampling stays robust under diverse conditions.

TARGET HARDWARE

GPU: NVIDIA® GeForce GTX 1660 SUPER (6 GB GDDR6, 1,408 CUDA cores).

CPU: Intel® CoreTM i7-10700 (2.90 GHz, turbo-boost, hyperthreading).

SOFTWARE STACK

C++ SYCL-based AdaptiveCpp/HipSYCL, with LLVM-IR JIT forkernel compilation.

RESEARCH MOTIVATION

Exact probability computation becomes intractible for large systems or complex scenarios. Alternate strategies are needed for evaluating large-scale PRA models.

RESEARCH OBJECTIVE I

Develop an efficient scheme for encoding linked event trees and fault trees as unified probabilistic tractable graphs, also known as probabilistic circuits.

RESEARCH OBJECTIVE II

Build a vectorized, data-parallel boolean function evaluator using hardware-native bitwise operations. Develop Monte Carlo sampling schemes for this evaluator.

RESEARCH OUTCOME

(1) Improved accuracy, as compared to alternative approximate methods. (2) Quantify risk models with hundreds of thousands of components, and millions of failure combinations. (3) Runtime speedup for comparatively smaller models.

LIMITATIONS & ONGOING WORK

Rare-events are significantly underepresented. Sampling correlated or dependent events requires additional implementation. Scaling studies that challenge accuracy, throughput, and model size are underway.